The recitations of the amended claims, new claim 10, and the dependent claims are believed to be allowable. The dependent claims are believed to be allowable at least for depending from an allowable independent claim. Further, applicants do not believe that the Official Action has shown that all the features of the dependent claims are taught or suggested by the applied art.

Independent claims 1 and 2 have been amended reciting, in both claims, that the diffusion layer form a diffusion line extending, in a complete device, between adjacent memory cells.

Independent claim 10 recites that the diffusion layer of each of the transistor cells are of the same width and form diffusion lines extending, in a completed device, between adjacent memory cells.

Independent claim 2 has been further amended to recite that the shielding electrode extends in parallel with the floating gate and extends between plural memory cells in the completed device.

See on page 1 of the specification that this invention concerns a method of manufacturing a semiconductor device wherein a buried diffusion layer serves as a signal line. More specifically, see on specification page 8, the first full paragraph under the SUMMARY OF THE INVENTION heading, that an object of the present invention is to provide a device that is free of variations in width of the buried diffusion layer

disposed adjacent the floating gates.

The applied reference is not concerned with this type of structure or with the problem being addressed by the present inventors. Accordingly, the amended claims are not anticipated, nor rendered obvious by the applied art. In view of the below remarks, reconsideration and allowance of all the pending claims are respectfully requested.

Relevant to the rejected claims, BERGEMONT discloses a contactless flash EPROM cell array structure that includes polysilicon isolation blocks, and a process for its fabrication. The BERGEMONT device does not provide:

diffusion layers that are all of the same width;

diffusion layers that form diffusion lines extending (in a completed device) between adjacent memory cells; or

a shielding electrode running adjacent the floating gate and between plural memory cells in a completed device.

See Figure 10 showing that BERGEMONT provides isolation blocks; Figure 9 showing that the diffusion layers are separated not forming diffusions lines extending between adjacent memory cells; and Figure 11 showing that the diffusion layers are not all of the same width. This is because BERGEMONT concerns a different device structure and manufacturing concerns than does the present invention.

The disclosed BERGEMONT processes teach that a stacked structure is masked and patterned to define a plurality of

parallel, spaced-apart poly 1 strips (the precursors of poly 1 isolation blocks 104).

Refer to Figure 9 which, together with Figure 10, illustrates the layout of the BERGEMONT EPROM cell array 100 without buried diffusion lines or shielding electrode lines.

Figure 10 shows the separate drains of adjacent cells share a common source and are separated from adjacent shared-source cells by poly 1 isolation blocks 104. The individual source regions do not connect, nor do the isolation blocks.

Accordingly, as the primary reference does not teach the features recited in the independent claim, it is requested that the anticipation rejection be withdrawn. Similarly, the obviousness rejection is requested to be withdrawn. Allowance of all the pending claims is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 23, the paragraph beginning on line 4 has been amended as follows:

--Then, as shown in Figs. 7A, 7B and 7C, an N-type impurity, for example such as arsenic ions is injected into the P-type semiconductor substrate 1 in a self-align manner with the use of the lower floating gate 4 and the device isolation shielding electrode 9 as masks.--.

IN THE CLAIMS:

Claim 1 has been amended as follows:

--1. (amended) In a method of manufacturing a semiconductor device comprising plural adjacent transistor cells provided with a gate electrode and a diffusion layer disposed adjacent to each of opposite end portions of said gate electrode, the method comprising the steps of:

forming a conductive layer on a semiconductor substrate through an insulation film;

patterning said conductive layer to form said gate electrode together with a shielding electrode, wherein said shielding electrode is disposed adjacent to each of opposite end portions of said gate electrode to extend in parallel with said gate electrode;

injecting an impurity into said semiconductor substrate in a self-align manner with the use of both said gate electrode and said shielding electrode as masks to form said diffusion layer [covering adjacent ones of transistor cells]; and

insulating said gate electrode in each of said transistor cells,

wherein said diffusion layer forms a diffusion line extending, in a completed device, between said adjacent transistor cells.--

Claim 2 has been amended as follows:

--2. (amended) In a method of manufacturing a nonvolatile semiconductor memory device provided with a plurality of integrated nonvolatile semiconductor memory cells each comprising: a lower floating gate; a control gate formed on said lower floating gate through an insulation film; a diffusion layer disposed adjacent to each of opposite end portions of said lower floating gate, the method comprising the steps of:

forming a first conductive layer on a semiconductor substrate through an insulation film;

patterning said first conductive layer to form said lower floating gate together with a device isolation shielding electrode, wherein said shielding electrode is disposed adjacent to each of opposite end portions of said gate electrode to extend in parallel with said lower floating gate between plural of said nonvolatile memory cells in a completed device; and

injecting an impurity into said semiconductor substrate in a self-align manner with the use of both said lower floating gate and said device isolation shielding electrode as masks to form said diffusion layer,

wherein said diffusion layer forms a diffusion line extending, in the completed device, between adjacent ones of said nonvolatile memory cells.--